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The New Millennium Program Microelectronics Systems Advanced Technology Development

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Abstract.

1. Introduction.

The purpose of the New Millennium Program is to accelerate the insertion of advanced space-related technologies into missions of the 21st century, using three deep-space and three Earth Oribiting technology validation spacecraft. By doing so, NASA is planning to enable a new vision of space exploration based on frequent, low-cost, and miniature scientific missions to the outer planets, as well as to Earth (reference NMP paper [NMP, 21stCentury]).

The technology development and validation efforts of the NMP are focused around six technology thrust areas: Spacecraft Autonomy, Telecommunications, Multifunctional And Modular Systems (MAMS), Micro Electro Mechanical Systems (MEMS), Instruments, and Microelectronics Systems. For each technology area, government-industry teams have been formed, and are refered to as Integrated Product Development Teams (IPDT). These teams operate in the form of government-industry consortia that develop and validate new enabling space-related technologies, in a cooperative and collaborative fashion.

In the following section, we first introduce the scope of the Microelectronics Systems IPDT as well as its current membership. In Section 3, we summarize the results of the IPDT technology roadmapping process, which will be descibed in detail in a subsequent publication currently in preparation [Roadmap]. In Section 4, we describe the technologies selected as well as the avionics architecture chosen for validation on the first NMP spacecraft, to be launched in January 1998.

2. Microelectronics Systems IPDT Scope and Membership

2.1 IPDT Scope

The scope of the Microelectronics Systems IPDT is broad, ranging from the lowest level such as semiconductor matierials, processes and devices, to the highest level such as spacecraft avionics systems. In between are electronics circuits, components, functional modules, and subsystems for:

1. Storage: static, dynamic, volatile, and non-volatile.
2. Processing: central processing units (CPU), micro-controllers, special-purpose processors such as digital signal processors (DSP), neural networks, systolic arrays, and other functional units such as Field Programmable Gate Arrays (FPGA), etc.
3. Input/Output: serial and parallel interfaces for communication between components, modules, and subsystems, as well as communication with analog devices, sensors, and actuators.

In common to all of the above listed components is the need for a drammatic reduction in the electronics mass, volume, and power dissipation, whereas maintaining the same growth trend towards higher functional density. That is, the NASA vision for space exploration in the 21st century requires the use of low-power, miniaturized, highly capable, reliable, and yet low-cost space avionics systems.

2.2 IPDT Membership

In order to meet this formidable technological challenge, NASA has formed the Microelectronics Systems government-industry team, whose membership is shown in Table 1, below. As can be seen, the government members are not only from NASA Centers (JPL, GSFC, and LeRC), but, also from the DOD Air Force Phillips Laboratory, MIT Lincoln Laboratory, and the Sandia National Laboratory. The industry partnres include Loral Federal Systems, TRW, Lockheed Martin, Boeing, Space Computer Corporation, Optivision, and Honeywell. In addition, three university collaborators were chosen: USC, UCSD, and Georgia Institute of Technology. In Table 1, we list the names of the IPDT members, the organizations they represent, and the technology areas they were chosen to represent during the technology roadmapping phase of the program development.

Member	Representing Government	Technology Focus

Leon Alkalai, Co-Lead	NASA/JPL	Data Processing/3D Packaging
Danny Dalton, Co-Lead	NASA/GSFC	Data Processing/Optical Communication
Ron Marx	AF/PL	Improved Space Computing
Craig Keast	MIT Lincoln Labs	Low Voltage/Semiconductors
Michael Knoll	Sandia National Labs	Semiconductor Technology
Jim Soeder	NASA/LeRC	Power Electronics
Member	**Representing Industry**	**Technology Focus**
Charles Chalfant	Optivision	Optoelectronics/MCMs
Abhijit Chaterjee	Georgia Institute of Technology	Design for Testability/Low Power, Low-Cost Packaging
Robert DeLean	Loral Federal Systems	Power PC flight computer
Gerhardt Franz	Lockheed Martin Corporation	Power Management, 3D Packaging
John Samson	Honeywell Corporation	Magneto-Resistive RAM, RH-ASIC technology
Warren Snapp	Boeing	Optical I/O, Mixed Signal ASICs
Nick Teneketges	Space Computer Corporation	3D MCM Packaging
Darby Terry	TRW	Solid State Recorders
Volkan Ozguz	UCSD	3D VLSI
Massoud Pedram	USC	Low Power Synthesis

Table 1: New Millennium Program Microelectronics System IPDT Membership

In the following section we summarize the technology development roadmap that the IPDT developed during a six month period between

May and November of 1995. This technology roadmap will be published as a separate document in the immediate future.

3. The Microelectronics Systems Technology Roadmap

Before we summarize the results of the Microelectronics Systems roadmap, it is useful to discuss what is meant here by a '*roadmap*' as well as the assumptions made during the'*roadmapping*' process. A technology roadmap, according to the Microelectronics IPDT, consists of two parts: i) a proposed technology vision in terms of a set of enabling capabilities and associated metrics, and ii) a time-series of data points originating with today's state of the art, and leading to the envisioned capabilities of the future. There are many reasons for qeustioning the rationale, objectivity, and assumptions behind a roadmapping process performed by a selected few. It is therefore, perhaps more appropriate to refer to the technology roadmap as a 'strategy' rather than a roadmap for achieving a proposed vision. An excellent example of a recent roadmapping activity completed by the Semiconductor Industry Association, is documented as the 1995 National Technology Roadmap for Semiconductors [Roadmap]. This document was therefore used as a starting point for the Microelectronics Systems IPDT technology roadmap, which was divided into seven different categories, summarized as follows:

1. Semiconductor Technology. The main goal here is to follow the impressive progress that the commercial CMOS technology has been making with regards to the reduction of the semiconductor feature size, density of integration, and power dissipation. In particular, the use of Silicon On Insulator (SOI) CMOS technology holds the potential for both low-operating voltage (and thus low power), and radiation tolerance. For the purpose of roadmapping the commercial semiconductor technology development, the SIA National Technology Roadmap for Semiconductors [Roadmap] was extensively used. For example, Table 1 summarizes the semiconductor technology evolution based on expected reduction in feature size using advance lithography processes.

[Insert Table here]

Table 1. SIA National Technology Roadmap for Semiconductors predicts feature size scaling for the next 15 years

2. Processors. In the area of general purpose processors, a long term decision was made to use commercial instruction set architectures for space applications. In particular, the Power PC architecture was selected due to its widespread use, availability of commercial off-the shelf (COTS) software, and development tools. For special purpose processors, Digital Signal Processors were roadmapped for future applications, as well as arrays of DSP for high-performance on-board computing applications.

3. Storage. Low-power high-capacity storage using commercial parts such as DRAMs for volatile, and Flash for non-volatile memory, was chosen as an enabling technology for future space applications. The roadmap actually did include many other magnetic storage technologies such as VBL, MRAM, FeRAM, etc. Non-Volatile Holographic storage is also part of the future roadmap.

4. I/O. High bandwidth low-power input/output technologies were identified as enabling for both deep-space and Earth Orbiting missions. For deep-space, 1-20 Mbps fiber optic networks are envisioned, and for Earth Orbiting missions, 1-2 Gbps Fiber Optic Data Buses using Asyncrhonous Transfer Mode (ATM) technology are consdiered.

5. Packaging. Advanced 3D microelectronics packaging is a major enabling technology for the dramatic reduction in spacecraft mass and volume. In this area, the use of 3D Multichip Module (MCM) stacking technology using vertical elastomeric interconnects is the proposed first step; followed by 3D High Density Interconnect (HDI) technology, and finally using 3D VLSI technology which reaches the physical limits of electronics device integration into the third dimension.

6. Engineering Design Automation. In this field, the use of high-level design tools, formal verification methods, and executable design specification, were elements of the technology roadmap. Moreover, low-power synthesis tools were chosen as the first step towards using EDA tools to reduce the overall spacecraft electronics power.

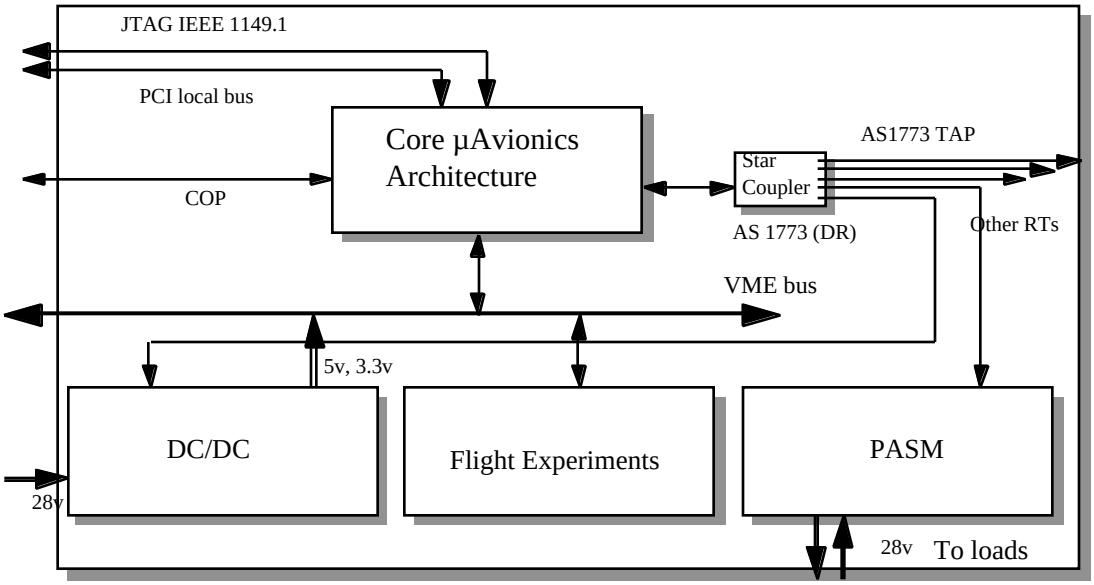
7. Power Electronics. The power electronics technology (which does not include power sources) is divided into two areas: 1) Power Conversion using DC/DC converters, and 2) Power Activation and Switching Modules (PASM). The first item develops the high-efficiency and highly integrated power conversion technology, and the latter encompasses integrated mixed signal technology for power switching.

4. NMP Deep-Space 1 µAvionics Architecture

The proposed spacecraft micro-avionics architecture for the first NMP mission (DS1) evolved from the technologies specified in the above summarized roadmap. The architecture is shown in the block diagram below. The architecture consists of four avionics modules that communicate over a standard avionics backplane bus (VME). The first module inccludes the 32-bit RISC processor, 2 Gbit of Solid State Recorder (SSR), 160 Mbytes of Extended Memory using 3D dis stacks, and Fiber Optic I/O links for communication with the spacecraft. Also shown in the Figure is a separate passive star-coupler used for inter-module communication using fiber-optical links.

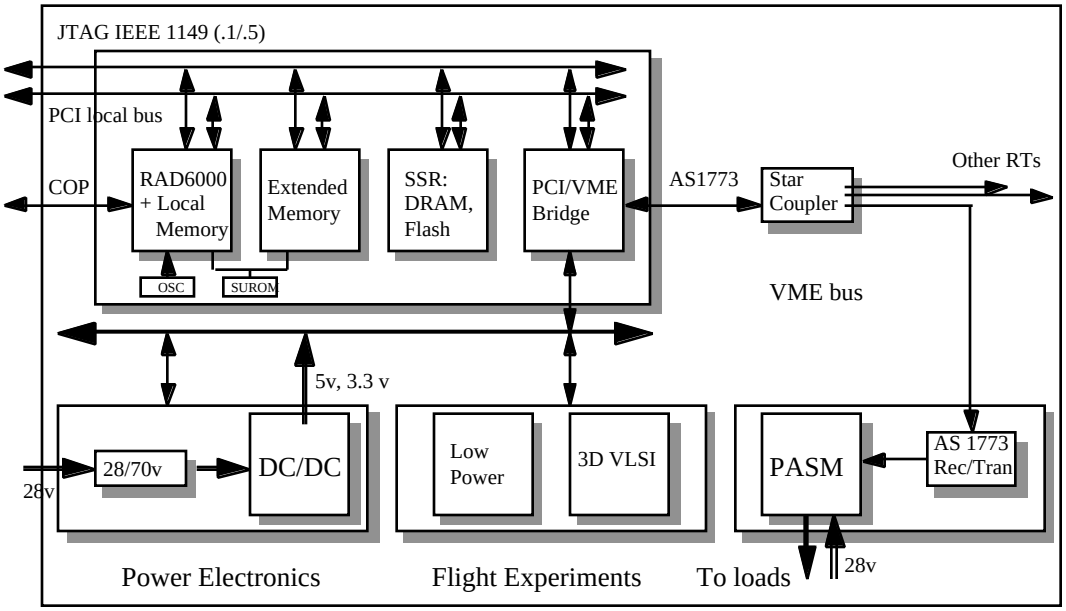
The second and the third modules, represent hte power electronics DC/DC converter and the PASM, and the fourth module contains several microelectronics experiments for both low-power and 3D VLSI validation in space. The principal investigators of these experiments are: MIT Lincoln Labs., UCSD, USC, and Georgia Institute of Technology.

Deep Space Flight 1 Core µAvionics High-Level Architecture



A more detailed block diagram of the proposed DS1 micro-avionics architecture is shown in Figure 2 below.

New Millennium Deep Space Flight 1 Core µAvionics Architecture



Of particular interest to the NMP Microelectronics IPDT was the design of a standard, low-cost spacecraft architecture discussed below.

Design for Low-Cost.

Since an important aspect of the New Millennium Program is to develop and accelerate the insertion of advanced space technology for the low-cost exploration of space, it is interesting to note the Microelectronics Systems IPDT approach towards this goal. From the above shown detailed block diagram, it is evident that the proposed architecture will achieve low recurring cost due to the following important attributes, which were set as guiding principles upfront:

1. Use components with commercial heritage.
2. Use standard Interfaces.
3. Use of commercial software development platforms.
4. Scalable architecture
5. General Purpose Design

Commercial Heritage. The proposed NMP architecture uses components with commercial heritage as the first choice, over space unique flight hardware or software. This is best illustrated by the following examples. First, the processor selected for the NMP long-term roadmap is the Power PC architecture (604 in particularly) which is widely used in the commercial industry. Moreover, NASA is collaborating together with the Air Force Phillips Laboratory to ensure the transfer of the commercial IBM Power PC fabrication line to a radiation hardened process at the Loral Federal Systems Division. Second, TRW is developing the Solid State Recorder module using exclusively commercial 16 Mbit DRAM and 16 Mbit Flash die, stacked in 3D to achieve high volumetric efficiency of silicon.

Standard Interfaces. Perhaps even more important than the use of commercial components wherever acceptable, it is important to use standard interfaces for inter-module communication, system testing, etc. In the DS1 architecture, the following standard interfaces are being used:

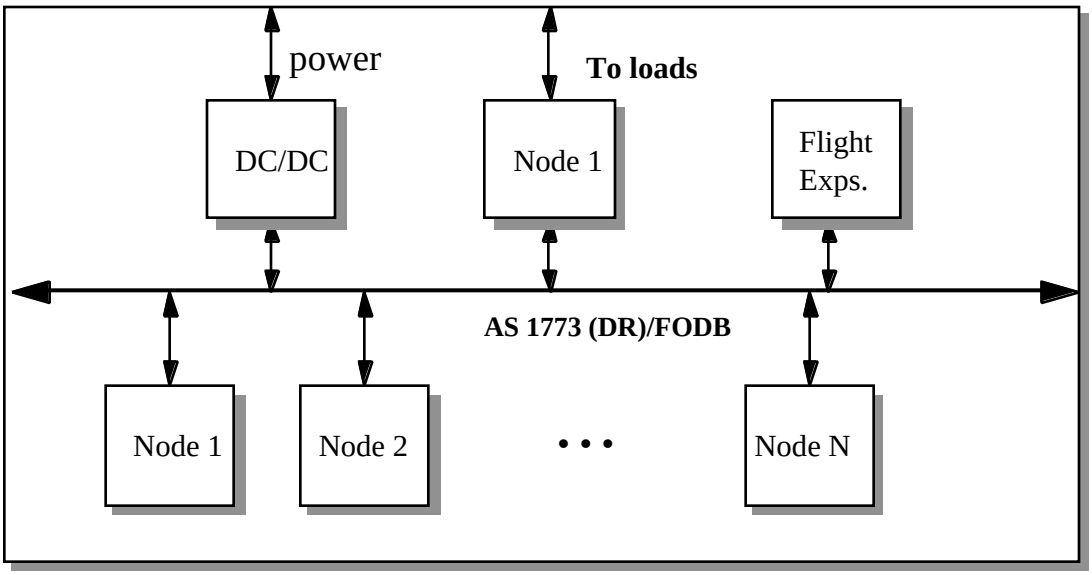
VME	Avionics standard backplane sub-system bus
PCI	Peripheral Component Interconnect, a commercial local bus standard
JTAG	IEEE 1149.1 Standard Test Access Port architecture
AS 1773	Avionics standard serial fiber optic bus: dual rate and dual redundant

Commercial Development Platform . The run-time environment of the proposed DS1 architecture includes the commercial VxWorks Operating System, the C programming language and compiler, and a set of off-the-shelf development tools that operate on Unix workstations. Therefore, many program development and software debugging tools are available for this development environment and prototyping platform.

A Scalable, Distributed Architecture . Having an architecture that scales is attractive since it can potentiall address a broader community of users, and thus further reduce the overall recurring cost, and further ammortize the non-recurring cost. Moreover, applications such as on-board spacecraft autonomy and on-board science data analysis require higher degrees of on-board computing capabilities that can be offered by any single processor. Therefore, a multiprocessor architecture that can offer higher computation throughputs and higher degrees of system reliability (due to redundancy) are extremely attractive.

A simple extension of the proposed DS1 NMP avionics architecture towards a distributed architecture is shown in the figure below. In this architecture, single avionics nodes like the one previously detailed, are connected over a spacecraft Local Area Network which in fact can either be the currently used AS 1773 bus, or the future roadmapped high bandwidth Fiber Optic Data Bus (FODB). An architecture like this is attractive for the following reasons: First, it is simple. It resembles a distributed LAN architecture that most engineers understand, and use in their office environments. Second, it is a simple extension of the single node architecture, where information between nodes is exchanged via message-passing protocols. Third, it enables higher levels of system reliability due to the possibility for system level redundancy. That is, if one node failes, any other node can pick up the load and continue operatng despite failures. And finally, this architecture is attractive since it is easy to emulate. In fact, a Power PC workstation on a LAN is already most of what an engineer needs to start prototyping a target system.

New Millennium Microelectronics Systems
Distributed Architecture



General-Purpose. The proposed DS1 architecture was not intended to be unique for any specific type of space mission, but, in fact general purpose, and applicable to deep-space missins, Earth Orbiting missions, and planetary probes, micro-science statsions, and landers.

5. Detailed Technology Description

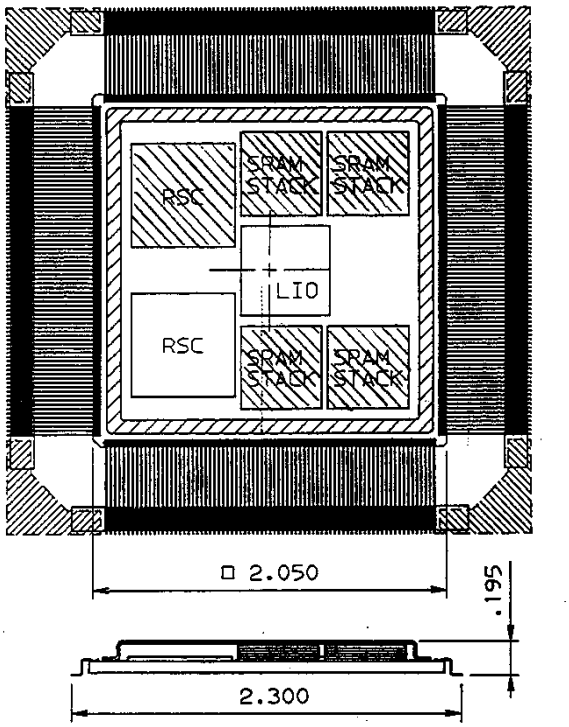
In this section, we present a more detail view of the specific technolgoy slices that are being integrated into the spacecraft 3D micro-avionics architecture. These slices (a total of four) are listed as follows:

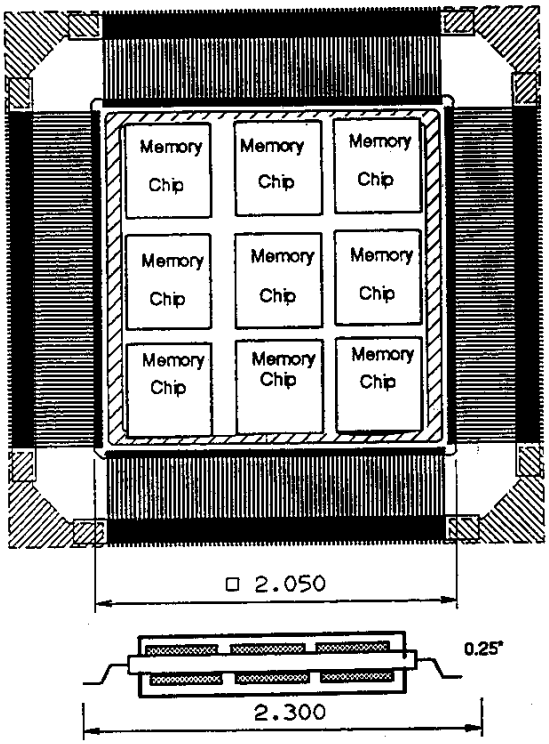
1. Processor Slice.
2. Extended Memory Module.
3. Solid State Recorder Module.
4. I/O Module

All four modules are stacked together using a low-cost flexible, MCM stacking technology, described in the following seciton.

5. 1 Processor Module.

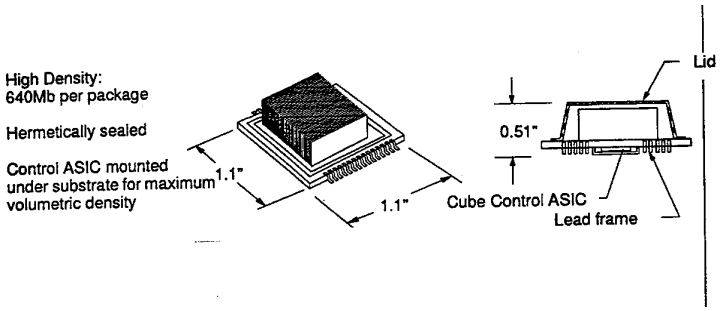
The processor slice consists of two Multichip Modules: a RAD6000 ISA processor module designed for lock-step-compare; and a high-bandwidth memory module. Both modules use only radiation hardened components, and are packaged in 308 pin CQF packages. The MCM technology used is an MCM-D technology refered to as VCOS (vertical chip on silicon). The die attach process is flip-chip, which has been used extensively by Loral.
Both MCMs are shown in the figure below.





5.2 Extended 3D Memor Module

The extended 3D Memory module provides 160 Mbytes of directly addressable DRAM space to the flight computer. This amount of storage is achieved within a very small volume and foot-print by using advanced 3D die stacking technology, as shown in the figure below. Two stacks are actually icluded in the same MCM module together with an DRAM controller module.

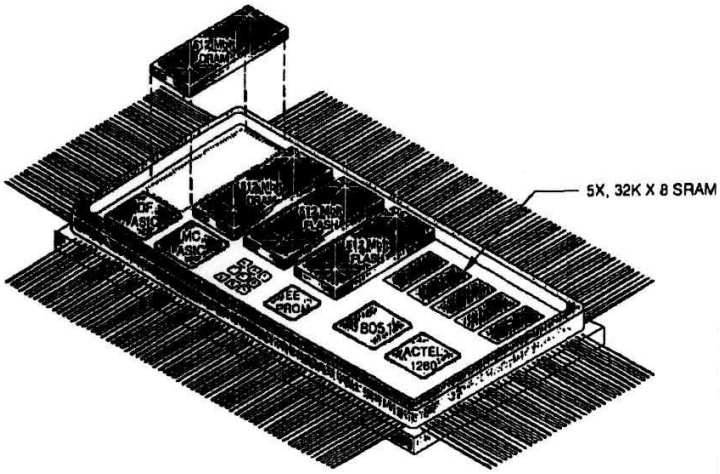


5.3 I/O Module

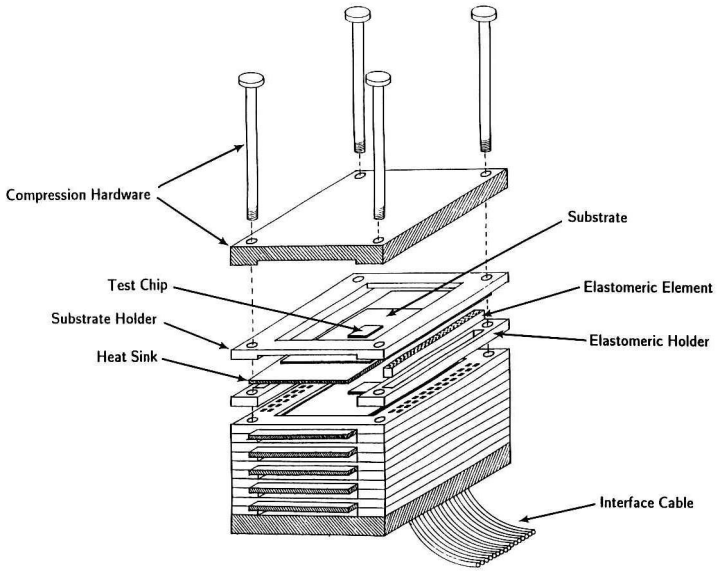
The I/O module, designed by Boeing, includes all the interface logic needed to translate from the VME to the PCI local bus, and from the PCI bus to the spacecraft serial bus, the AS 1773. The interface logic is packaged in a single MCM without the actual physical transcievers. These are outside the actual MCM. The MCM technology used is the MCM-C technology (or thick film ceramic technology).

5.4 Solid State Recorder Module.

The SSR module by TRW, uses agressive 3D stacking techniques to achieve high levels of integration. That is, the SSR has a total of 2 Gbit of starage. Half is DRAM based, and the other half is Flash based. The proposed combination meets the spacecraft system requirements for non-volatile and volatile storage.



5.5 3D Multichip Module Stacking Technology.
The proposed 3D MCM packaging technology has been developed and prototpyed by a small business in Santa Monica, called Space Computer Corporation. In the figure sown below, MCMs are mounted on PCBs, which are then stacked in 3D, using elastomeric devices with embedded wires for inter MCM communication.



Upon integrating the four spacecraft avionics slices into a single four-layer system, it is then mounted onto a VME board for further

integration into the Avionics Electronics Module, and then subsequently into the DS1 spacecraft.

6. Conclusions

In this paper, we have summarized the results of the technology roadmapping effort performed by the NMP Microelectroncis Integrated Product Development Team (IPDT) during a five month period between May and November 1995. As a result of this roadamp, a low-cost, 3D Micro-Avioncs architecture has been proposed, which uses only existing and commercially acceptable standards for inter-module interface. This highly integrated module will provide the main spacecraft control and data handling functions for the first NMP deep-space mission. Moreover, the architecture is general, and can be used as well for Earth Orbiting missions, as well as for other space related applications, such as commercial remote sensing and glabol communication.

7. References:

[NMP] K. Casani and B. Wilson "*The New Millennium Program Plan*", JPL document".

[SIA] "*The National Technology Roadmap for Semiconductors*", Semiconductor Industry Association, San Jose, CA 95129, 1995.

[Roadmap] "Microelectronics Systems Technology Roadmap for the NASA New Millennium Program", edited by Mark Underwood and Leon Alkalai, document in preparation, Jet Propulsion Laboratory, California Institute of Technology, CA 91109.

[21st Century] Freeman J. Dyson, "21st Century Spacecraft", Scientific American, September 1995.

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